## REMARKS

Claim Rejections Under 35 USC 103(a)

Claims 25-29 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. '461 (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

Claims 30-34 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. '461 (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

Claims 35-39 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. '461 (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

Claims 47-51 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. '461 (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

Claims 52-53 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. '461 (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227) and Pedder (US Patent No. 5,717,245).

The rejections under 35 USC §103(a) are respectfully traversed for the reasons to follow.

Summary of the Invention

The claims are directed to a "semiconductor component". In the elected embodiment of Figures 1-7, the component can comprise a chip module 24 (Figure 2E), a multi chip module 28 (Figure 3) or a semiconductor package 72 (Figure 7). In each case, the component includes a substrate 10 (Figure 2) and a blanket deposited conductive layer 14 (Figure 2) on the substrate 10. In addition, the component includes conductors 16 (Figure 2) on the substrate 10, and a semiconductor die 20 (Figure 2E, 3A or 7) in electrical communication with the

conductors 16. The die 20 can be "flip chip" mounted as shown in Figure 2E, or "wire bonded" as shown in Figure 3A.

Each conductor 16 is defined by a pair of laser machined grooves 15 (Figure 2) in the conductive layer 14. As shown in Figure 2C, the conductors 16 comprise portions of the conductive layer 15 separated by the grooves 15 and by remaining portions of the conductive layer 15. As shown in Figure 4, the grooves 15 are laser machined using a laser 44 and a base 48 configured to move the substrate 10 in X and Y directions.

In addition, as shown in Figure 2, each conductor 16 includes a bond pad 18 (contacts) configured for flip chip mounting or wire bonding the die 20. Each conductor 16 can also include a contact pad 22 (contacts) configured for electrical connection to outside circuitry. In the case of wire bonding, an opening 40 (Figure 3A) can be laser machined in the conductive layer 14 for attaching the die 20 to the substrate. As shown in Figure 5A, the substrate 10BGA can also include conductive vias 58 in electrical communication with the conductors 16BGA, and contact balls 66 in electrical communication with the conductive vias 58.

**Argument**

MPEP 2142, 2143 set forth the three basic criteria for establishing a prima facie case of obviousness under 35 USC §103(a). First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success in obtaining the claimed invention based upon the references relied upon by the Examiner. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicant submits that the cited art does not teach or suggest all of the present claim limitations, such that the

third criteria of the above MPEP rule has not been met. A first limitation of the present claims not disclosed by the art is conductors 16 (Figure 2) on the substrate 10 (Figure 2) defined by laser machined grooves 15 (Figure 2) in a conductive layer 14 (Figure 1A). In this regard the Frankeny et al. reference has been cited as teaching:

"using conventional laser drilling or punching of metal (Fig 5; Col. 5, line 63-Col. 5, line 9) to define a plurality of conductors/contacts (98 in Fig. 5) through the conductive layer (copper layer in Fig. 5) where the conductors comprise portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer."

This interpretation of Frankeny et al. is incorrect, as the conductors 98 are not formed by laser machining grooves in a blanket deposited conductive layer, but rather are formed by plating, photoimaging and etching techniques. As stated at column 6, lines 3-8 of Frankeny et al.:

"Circuitization of the substrate is accomplished by traditional plating, photoimaging and etching techniques common to printed circuit board manufacture. The finished circuit card would have a construction as shown in Figure 5 with metal 98 applied through both electrically isolated and groundplane vias.(underlines added)"

Admittedly Frankeny et al. teaches a "laser drilling operation" at column 5, line 65 to form "another via" (e.g., isolated via and ground plane via in Figure 5). However, the copper layer in Figure 5 of Frankeny et al. is plated and etched after formation of the vias, such that laser machining of a planar conductive layer is not suggested. In addition, although laser drilling of vias is known in the art, laser machining of grooves in a planar conductive layer to form conductors is not suggested by conventional laser drilling techniques.

Pedder teaches a semiconductor package 10 having a substrate 12 which comprises separate metallization layers 30, 31, 32 (Figure 3). As stated at column 4, lines 11-18 of

Pedder a metallization pattern (microstrips) are formed using a "screen printing process". With such a process, there is no remaining conductive layer on the substrate as presently claimed. In addition, Pedder teaches "laser or abrasive trimming" of the microstrip pattern at column 7, lines 3-4 "to adjust the length and resonant behavior of the line".

However, with the Pedder laser trimming process, there would be no laser machined grooves in a conductive layer which define the microstrips (conductors) as presently claimed. Rather, only the length of the microstrips (conductors) is laser trimmed, and the width is conventional. The laser machined microstrips in Pedder thus have a different structure than the conductors presently claimed.

In addition to the limitations on laser machined conductors not being taught by the art, other limitations of the present claims are also not taught by the art. In particular, independent claims 25 and 52 include recitations of a "conductive via" through the substrate, in combination with laser machined conductors on a surface of the substrate. Although conductive vias are known in the art, the combination of conductive vias and laser machined conductors is not suggested by the art.

Further, independent claim 35 includes the limitation of "the thickness of the conductive layer, and a width of the conductors selected to provide a selected impedance for the conductors". Although the conductors in Hembree et al. inherently have a width and a thickness, there is no suggestion of selecting the width and the thickness to provide a selected impedance.

Still further, independent claim 30 and 47 include recitations of the laser machined grooves being formed "through the thickness of the conductive layer extending on the surface in a first direction and in a second direction". Antecedent basis for these recitations is contained in Figures 2, 2B and 4, and by the description at column 10, lines 12-21 of the specification. The first and the second

directions refer to the X and Y directions of Figure 4. Although laser machining has been used in the art to form conductive vias in the Z direction as in Frankeny et al., or in one direction as in Pedder, laser machining has not heretofore been used in two surface directions to define conductors on the surface.

## Conclusion

In view of the above amendments and arguments, favorable consideration and allowance of claims 25-39 and 47-53 is requested. An IDS is also being filed with this Amendment. Should any issues remain, the Examiner is asked to contact the undersigned by telephone.

DATED this 3rd day of October, 2001.

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October 3, 2001
Date of Signature

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Marked Version Of Specification Showing Location of Changes

In the "Cross Reference To Related Applications" added by the Preliminary Amendment dated October 18, 1999 after "1998" --, add now US Patent No. 6,107,119--.

Marked Version Of Amended Claims

25. (twice amended) A semiconductor component comprising: [;]

a substrate having a first surface and an opposing second surface;

a conductive layer on the first surface;

a plurality of conductors on the first surface defined by a plurality of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated from one another by remaining portions of the conductive layer;

at least one semiconductor die on the first surface in electrical communication with the conductors;

a plurality of conductive vias [in] through the substrate from the first surface to the second surface in electrical communication with the conductors; and

a plurality of external contacts on the second surface in electrical communication with the conductive vias.

26. (twice amended) The semiconductor component of claim 25 further comprising a plurality of [bond] pads on the conductors [and] bonded to the semiconductor die.
[is wire bonded to the bond pads.]

27. (twice amended) The semiconductor component of claim 25 further comprising a plurality of [bond] pads on the conductors and wherein the semiconductor die is flip chip mounted to the [bond] pads.

30. (twice amended) A semiconductor component comprising: [;]

a substrate [comprising] having a surface;

a conductive layer on the surface having a thickness;

a plurality of conductors on the surface defined by a plurality of pairs of laser machined grooves through the thickness of the conductive layer extending on the surface in a first direction and in a second direction, each conductor comprising a portion of the conductive layer which is electrically isolated on either side by a pair of laser machined grooves; and

a semiconductor die on the surface in electrical communication with the conductors.

35. (twice amended) A semiconductor component comprising:

a substrate [comprising] having a surface;

a conductive layer on the surface having a thickness;

a plurality of conductors on the surface comprising portions of the conductive layer, each conductor defined and electrically isolated by a pair of laser machined grooves through the conductive layer; and

a semiconductor die on the substrate in electrical communication with the conductors;

with the thickness of the conductive layer, and a width of the conductors selected to provide a selected impedance for the conductors.

47. (amended) A semiconductor component comprising: [;]

a substrate [comprising] having a surface;

a conductive layer on the surface; and

a plurality of conductors on the surface defined by a plurality of pairs of laser machined grooves through the conductive layer extending in a first direction or a second direction on the surface, the conductors comprising portions

of the conductive layer which are electrically insulated from one another by the laser machined grooves, the portions of the conductive layer including first contacts on first ends thereof configured for bonding, and second contacts on second ends thereof configured for electrical connection to external circuitry; and

a semiconductor die on the substrate bonded to the first pads.

52. (amended) A semiconductor component comprising: [;]

a substrate having a surface;

a conductive layer on the [substrate] surface;

a plurality of conductors on the [substrate] surface defined by a plurality of first laser machined grooves through the conductive layer to the surface, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves;

a plurality of contacts on the conductors defined by a plurality of second laser machined grooves through the conductive layer to the surface;

a plurality of conductive vias [in] through the substrate in electrical communication with the conductors; and

a semiconductor die on the substrate in electrical communication with the contacts.